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Design and computational modeling of fault current limiter topologies

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Abstract: The increase in demand for electric power and the insertion of a distributed generation led to the rise of the short-circuit current in substations. Most of these Brazilian substations were designed decades ago, because of that their equipment may not support the new short-circuit current levels. To protect the installed equipment and avoid excessive costs replacing old devices, it is possible to install Fault Current Limiters (FCLs). This document is a report from an R&D project that evaluated FCL topologies considering real parameters in simulation from used equipment, concluding that the selected FCL topologies accomplished their technical objective. However, before implementing these topologies in the distribution system, one should consider the technical and economic feasibility of using semiconductor switching devices.

Keywords: Short Circuit Current Limiter, Resonant Circuit, Series Switched Inductor Circuit, Fault Detection

1. INTRODUCTION

In recent years, world energy consumption has grown fast and is projected to increase by 28% until 2040 (EIA, 2017). In Brazil, the energy consumption in 2017 was 1.2% higher than in the previous year (EPE, 2018). As power generation does not grow at the same rate as demand, the system is forced to operate close to its maximum capability, leading to highly active and reactive power flows. This operational condition implies higher transient currents in the distribution system lines during a short circuit. Since many Brazilian substations were built a few decades ago, the new levels of short circuit current have already overcome the maximum capability of protection devices (Prigmore and Schaffer, 2017).

To mitigate this problem, a Fault Current Limiters (FCLs) can be inserted between the transformers and the distribution lines (Castro et al., 2018; Kozak et al., 2017; Sahebi et al., 2017). This solution is less costly than replacing the protection devices.

In many situations, short circuits can cause more problems to the electrical network than just the discontinuation of the power supply. For example, it can damage several equipments in the substations. To avoid such damages, FCLs can be installed in distribution system substations, where high rates of equipment burn are detected due to the occurrence of faults (Badakhshan and Mousavi G., 2018).

FCLs are usually placed in series with the power grid, preventing the electric current from exceeding system limits during the occurrence of faults. The literature presents several FCL topologies and the choice of the best type to be installed in a given system must be based on technical and economic criteria (Castro et al., 2018).

This document is a report from an R&D project entitled "Hybrid Short Circuit Current Limiter for Distribution Systems" executed by Federal Fluminense University (UFF in Portuguese) in partnership with the local distributor Light S/A. This manuscript presents the basic design and computational modelling of two different fault current limiter topologies. Simulations were performed using the software ATPDraw, which is the graphical interface of the Electromagnetic Transients Program (EMTP).

2. BASIC PRINCIPLES OF THE STUDIED FCLS TOPOLOGIES

The two FCL studied in this work were named Series Switched Inductor (SSI) and Resonant. This section presents its basic principles.

2.1. SERIES SWITCHED INDUCTOR

This type of FCL was also studied in (Abramovitz and Ma Smedley, 2012; Ahmed et al., 2006; Chen et al., 2006; Genji et al., 1994; Meyer et al., 2004). It is composed of an inductor in parallel with a switch, as presented in Fig. 1. The switch is closed in the normal operation of the system and should be opened during the fault. At this moment, the current will be limited by the inductor's impedance. The component values used in simulation were L = 0.314 mH and RJ = 0.02 Ω.

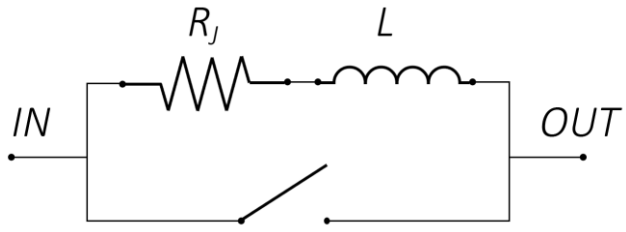

Fig. 1. Series Switched Inductor topology.

2.2. RESONANT

This type of FCL has a switched capacitor in series with an inductor. The circuit resonates when the switch is opened like presented in (Karady, 1992; Martins Lanes et al., 2007; Sarmiento, 2007; Sugimoto et al., 1996) and illustrated in Fig.

2. During the occurrence of a short circuit, the capacitor is removed from the system, and the inductor limits the current. The component values used in simulation were L = 0.314 mH, C = 22.408 mF, RC = 10 kΩ and RJ = 0.01 Ω. The RC and RJ elements represent the capacitor discharge and Joule effect resistances, respectively.

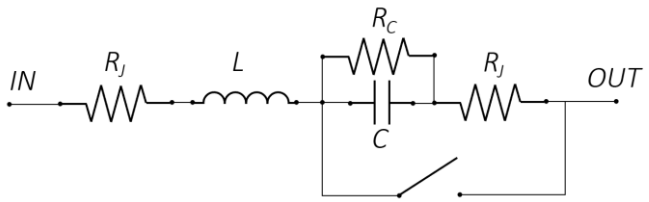

Fig. 2. Resonant topology.

3. Semiconductor Switch Model Description

The model of semiconductor devices in ATPDraw is a challenge since this software has only ideal devices in its library. This section describes how these devices were modeled in order to present a behavior closer to real. Two kinds of semiconductor devices were considered: Thyristors and IGBTs.

A bi-directional switch based on thyristors can be built in ATPDraw by connecting two of those elements in antiparallel, as can be observed in Fig. 3. The pulses generated by the "Command" enter the gate of the thyristors (highlighted in blue) and determine its state of conduction, where the opening will only occur when the current passes through zero, a typical characteristic of this type of switch. The elements R_{SW} and L_{SW} represent the resistance and inductance of a real model switch, respectively, to simulate their effects. Points 1 and 2 correspond to the terminals where the switches will be connected to the FCL circuit.

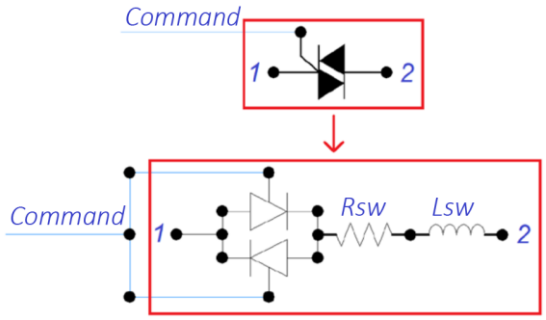

Fig. 3. ATPDraw Thyristor model.

Fig. 4 shows the modelling of the IGBT switch, also with R_{SW} and L_{SW} presented in its equivalent circuit, connected between terminals 1 and 2. A TACS switch was used in ATPDraw to simulate the commutation of the IGBT accordingly to the command signal on the gate. It is worth mentioning that this modelling is equivalent to two IGBTs in anti-series. The current passing through this switch represents both positive and negative half-cycles.

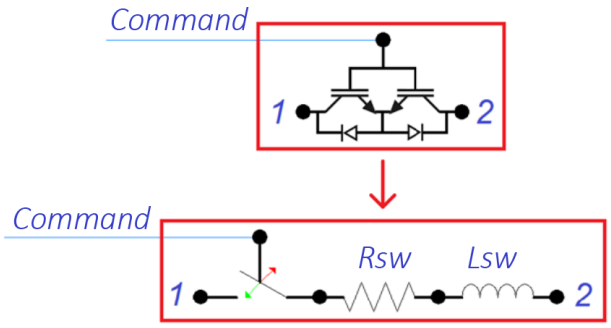

Fig. 4. ATPDraw IGBT modeling.

4. Simulated System Description

The modeled system consists of a 10 V_{RMS} AC voltage source at a frequency of 60 Hz which supplies a nominal Z_{LOAD} impedance (composed of a 1.25 Ω resistor and an inductor of 1.83 mH), the nominal current (I_{NOM}) being 7 A_{RMS}. To analyze the limiter's performance during a short circuit event the FCLs are connected to the voltage source through a small resistance (R_{SOURCE} = 1 μΩ) and in series with Z_{LOAD}, shown in Fig. 5. The short-circuit impedance Z_{SC} in parallel with Z_{LOAD} is composed of a resistor of 4.9 mΩ and an inductor of 0.19 mH.

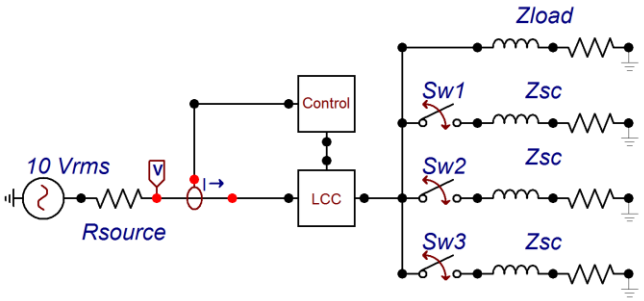

Fig. 5. ATPDraw system modeling.

The occurrences of the short-circuit events are generated by closing the switch 1, 2 and 3 (Sw1, Sw2 and Sw3) without de FCL at different times, where the voltage angle (θ) is equal to 0°, 45° and 90° respectively. After 100 ms of the duration of each short circuit, these are ended by the opening of Sw1, Sw2 and Sw3 also for θ equal to 0 °, 45 ° and 90 ° respectively. The results of these events are called the prospective current, which is the short-circuit current of the system that would be obtained when there is no actuation of the limiting equipment. The purpose of this sequence of events will be to evaluate the minimum, average and maximum values of currents and transient voltages that may occur during the fault. Also, these operations will be used for validation of the control system (proposed in the following section) in correctly identifying/distinguishing normal and short-circuit conditions.

5. Control System

For the elaboration of the control algorithm of the FCLs, the following initial information must be entered by the user (input data): the maximum value of the current module (limax1) from which the FCL will act in [A]; the value of the nominal system voltage (V_N) in [V_{RMS}]; the equivalent

impedance of the FCL (Z_{LIM}), in steady state [Ω]; the initial state of the switch (State) for normal operating condition of the system (0 open, 1 closed); the number of samples (ST) measured per cycle by the control system; the minimum time (time) of sample verification, after system normalization [ms]. For the simulation performed in this report, based on the system circuits and the modelled FCLs described in the previous sections, the input data is shown in TABLE I for each proposed FCL.

TABLE I. Control Parameters

Parameters	SSI	Resonant
limax1	50	
V_N	10	
Z_{LIM}	0,120053	0,1184
State	1	0
ST	256	
time	0,01667	

The flowchart of Fig. 6 shows the logic and dynamics of the control system, described through an algorithm in MODELS. The control logic implemented for fault detection takes into account the value of the current of the network and its derivative so that the fault must be detected before the current of the system reaches high values. The control system operates the switch contained in the FCL circuit as a function of the total current of the line measured at the input of the limiter (I), as shown in the equivalent circuit of Fig. 5.

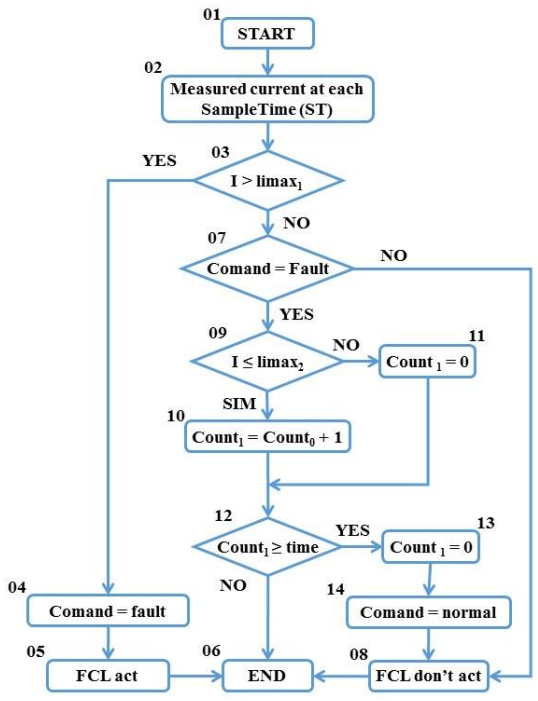

Fig. 6. Control flowchart.

In the beginning, step 01 of Fig. 6, the FCL is considered to be under normal operating condition, and the input data were entered into the control system. The current value measured is acquired at each iteration performed by the control system at step 02, based on the ST informed by the user. This ST represents the time between one iteration and another of a microcontroller, to reproduce its effect in the simulations. In conditional 03, if *I* is higher than $limax_1$ (minimum threshold for the FCL to act, prior to the Z_{LIM} insertion), step 04 is initialized by changing the command from the switch to "state in short circuit ", causing the FCL to act (step 05), finishing the iteration of the algorithm (step 06).

If the measured current is less than or equal to $limax_1$ (conditional 03), in conditional 07, it is checked if the system was short-circuited (command in a short-circuit state) in the previous ST. If it was not, the system then indicates that there is no fault and sends the command to finalize the algorithm through steps 08 and 06. On the other hand, if it was short-circuited, then it is analyzed in conditional 09 if *I* is less or equal to $limax_2$ (the minimum limit for the FCL to continue acting, due to the Z_{LIM} insertion). This limit is calculated by the algorithm, based on Z_{LIM}, $limax_1$ and V_N. If conditional 9 is true, the counter of consecutive samples of currents less than or equal to $limax_2$ (Count) is initialized, in step 10, adding another to its sum obtained in the previous step. If not, Count is reset in step 11, because the system is still short-circuited ($I > limax_2$).

This counter is used to verify if the system is still short-circuited, until a minimum number of consecutive samples less based on the time of verification (time). If this occurs (conditional 12), the system is no longer in the short-circuit state ($I \leq limax_2$), Count is reset (step 13) and the switch command is changed to "normal state" (step 14), causing the FCL to stop acting (step 08), terminating the algorithm (step 06). This counter is also used to identify if the system is in a fault condition through the numerical derivative of the current, allowing faster detection without necessarily obtaining a very high current.

6. Results

The results were obtained through simulation of the EMTP/ATP program, through the ATPDraw interface. The main parameters analyzed were: short-circuit current (or prospective); limited current; and the transient effects on the switch (di/dt).

Fig. 7 shows the results for the FCL SSI topology. It can be noted that using thyristor for this type of FCL the first peak of the limited current coincides with the prospective. This is because the thyristor performs the opening (0 state) only when the short-circuit current goes through zero, and so without limiting the first peak. After its actuation, the series inductor starts to limit the subsequent peaks. It also shows the results of the limiter if the thyristor is replaced by an IGBT switch, giving a reduction already at the initial peak of the first short circuit. This is due to the difference in the performance of the IGBT when compared to the thyristor, since there is no need to wait for the current to go through zero to change the state of the switch (aperture). The remaining peaks in the steady state had very close results for both switches. Small differences are justified by the reduction of the homogeneous portion caused by the limitation already in the first half cycle with the IGBT switch. It is possible to verify that the application of IGBT switch would be more appropriate for this topology, since it limits the short-circuit current already at the

first peak of the short-circuit current, due to its shorter response time to act.

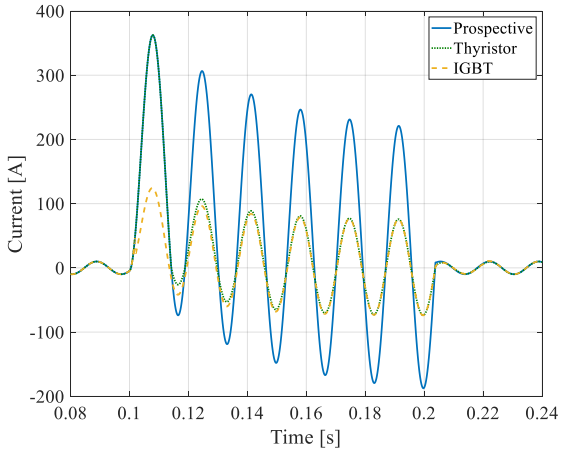

Fig. 7. Prospective and SSI current system with thyristor and IGBT.

Fig. 8 shows the current passing through the thyristor and IGBT during short-circuit. For the thyristor the current would reach 362.52 A and a di/dt of 0.052 A/µs. Using the model TT120N16SOF as a parameter it can be seen that this event would not damage the switch, since it can handle a current up to 2250 A for 10 ms and 140 A/µs. As for the IGBT, current goes up to 50 A and a di/dt of 0.006 A/µs. Using model BSM150GB60DLC as a parameter, it can be seen that this event also would not damage the switch since it can handle a current up to 300 A for 1 ms and 5600 A/µs.

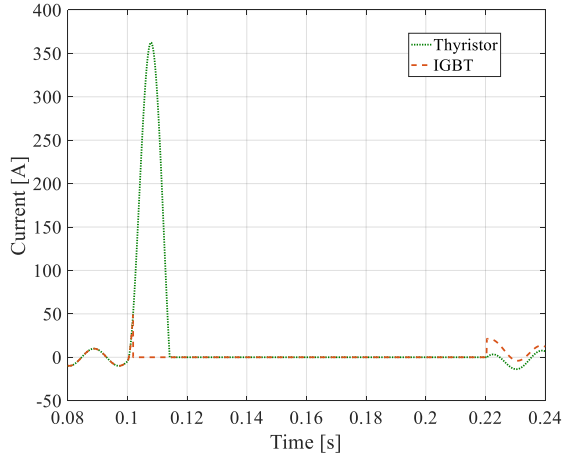

Fig. 8. Current through thyristor and IGBT in an FCL SSI topology.

Fig. 9 shows the result of Resonant FCL operation. In this topology, both thyristor and IGBT limited the current in the first peak. This effect is because that thyristor can change from open to close as fast as the IGBT. This demonstrates that for this FCL model, the type of applied switch does not influence in limiting the current since the operation is based on the closing of the switch, not on opening.

Fig. 10 shows the current passing through the thyristor and the IGBT. It can be seen that in this FCL the limited current goes through the switch, even for a short period. Using the parameters of the thyristor TT120N16SOF and the IGBT BSM150GB60DLC can be verified that both switches would not be damaged since it can handle a current of 120 A_{RMS} and 150 A_{RMS} respectively. For the di/dt simulation results in a 1.1 A/µs, a value that is below the maximum rating in both models.

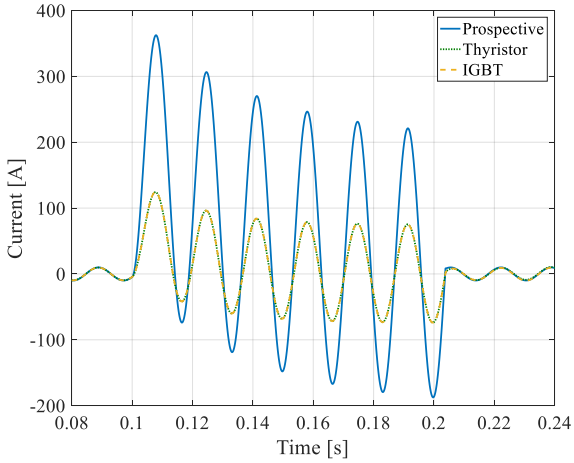

Fig. 9. Prospective and Resonant current system with thyristor and IGBT.

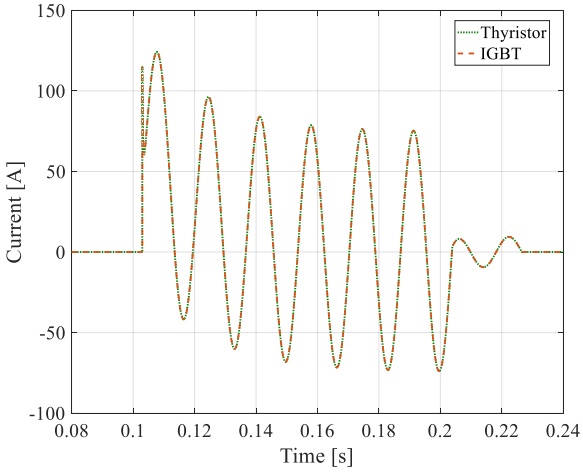

Fig. 10. Current through thyristor and IGBT in an FCL Resonant topology.

TABLE II summarizes the average percentual current reduction in all three fault angles considering the first and second peak. It is worth notice that the SSI with thyristor did not limit the current in the first peak and for Resonant topology both switches limited in the same level.

TABLE II. PERCENTUAL CURRENT REDUCTION IN ALL TOPOLOGIES AND ANGLES

Angle	Percentual Current Reduction			
	SSI		Resonant	
	Thyristor	IGBT	Thyristor	IGBT
0	65,0%	67,1%	67,2%	67,2%
45	64,4%	66,2%	65,7%	65,7%
90	63,0%	63,4%	62,0%	62,0%

7. CONCLUSION

According to the results obtained so far, it was verified that the SSI FCL with thyristor was not able to limit the short-circuit current in the first peak. Concerning to the SSI FCL with IGBT, it was found that the short-circuit current was

limited already in the first peak, since this switch does not require that the current pass through zero to open, thus enabling its future application in the next stages of the project.

It was also observed that the Resonant FCL, regardless of the type of switch used, presented closer values in the short-circuit current limitation, both for the first peak and for the subsequent peaks, being considered promising for the execution of prototypes in the following steps. Another advantage of this topology is the possibility of being used as a correction of power factor, with the proper switching of the capacitor.

The simulations showed that the stipulated switch models are suitable for future prototype tests. In this way, the selection of the FCL topology to be applied in the future should take into account, in principle, the technical characteristics and costs between the thyristor and IGBT.

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