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# A New Bidirectional Three-phase Neutral Point Clamped (NPC) Grid-Connected Converter: Analysis and Simulation ⋆

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**Abstract:** This paper deals with the theoretical development, analysis, and simulation of the new topology of three-phase NPC (Neural Point Clamped) converter. The proposed 6-kW three-phase converter is connected to a three-phase electrical network and due to its bidirectional characteristics can either send energy to the grid or receive it from the grid. The classic strategy of vectorial control at the DQ synchronous reference frame, along with a simple algorithm for Unit Vector Generation (UVG), have been employed to control the line currents in the grid and the DC-bus voltage, thus substituting the PLL (Phase Locked Loop). A PWM (Pulse Width Modulation) strategy is presented in the form of an analog circuit and used for switching the semiconductors in the converter. The obtained results were verified using Matlab/Simulink software. The proposed converter has five voltage levels at the output for each phase and proven more advantageous than the conventional NPC. In addition, it was obtained a better harmonic content in the grid currents because there is very low Total Harmonic Distortion (THD) both when acting as a rectifier and as an inverter.

*Keywords:* Neutral Point Clamped; Unit Vector Generation; Phase Locked Loop; Pulse Width Modulation.

## 1. INTRODUCTION

AC-DC/DC-AC converters are widely used in various applications such as AC drives, high voltage direct transmission (HVDC) systems, as well as in a few renewable energy applications (Bhat and Agarwal, 2008). Traditionally non-controlled rectifiers, such as those used in AC-DC converters or DC-AC inverters present a few problems, like harmonic current circulation, and the reactive component of the current from or to the source, thus generating highly non-linear characteristics. Harmonic currents generated by these non-linear loads can cause voltage distortion and may lead to operational problems in come sensitive equipment or other consumer products (Rashid, 2017; Bose, 1986).

With the advance of power electronics several multilevel inverter topologies have been presented and developed in the last few years for diverse applications, such as single-phase or three-phase NPC inverters, a three phase three-level inverter with flying capacitor, an H-bridge converter in cascade, and a modular multilevel converter (Rodriguez et al., 2002). These types of converters allow for higher output voltage as well as lower harmonic distortions.

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In order to provide a signal with higher output voltage levels, and in turn reducing the harmonic content of the AC current a new structure for a single-phase five-level NPC converter has been proposed for application in electric vehicle (Onar et al., 2012; Santos, 2013). The structure basically is a combination of the classic single-phase neutral point clamped topology with an additional leg containing two semiconductors allowing the voltage to be divided in two additional levels.

A novel 3-level VSC similar to that proposed (Onar et al., 2012) was introduced by (Soeiro and Kolar, 2011, 2012) as an alternative to many 3-level topologies (conventional NPCC, T-type VSCs, and A-NPCC) and the new solution proposed by (Soeiro and Kolar, 2011, 2012) can achieve not only higher efficiency than many typical 3-level structures, but can also overcome their drawback of extremely asymmetrical loss distribution for some operating conditions. The main difference between both topologies is that the topology proposed by (Onar et al., 2012) has a 5-level voltage at its output while that proposed by (Soeiro and Kolar, 2011, 2012) has a 3-level output voltage.

According to (Onar et al., 2012), the voltage rating applied to the semiconductor switches in the new single-phase

NPC inverter is much less than that of the H-bridge. Furthermore, this converter would be less expensive due to the reduced device ratings.

The grid interface topology proposed by (Onar et al., 2012) can also be scaled to three-phase applications, although it is originally a single-phase converter. To achieve a three-phase multilevel converter, one more leg (or bridge arm) should be added in parallel to the existing two phase legs. In a three-phase application, each phase leg should have two clamping diodes, whereas the number of capacitors at the dc link and their connections stay the same.

In this paper a new topology for a three-phase NPC converter is presented since the proposed converter has not yet been discussed in existing literature. The converter can transfer active power from wind energy, photovoltaic energy, chemical energy, or the energy storage system to the distribution network. In some cases, it also can transfer active power from the distribution network to the energy storage system as well as compensate reactive power to the network (Zhang et al., 2019). This study has been undertaken seeking to improve power quality, generating electrical energy with less distortion, and to propose an interface between three-phase loads (electric motors), renewable power supplies, and the electric network grid.

DQ synchronous reference frame vector control was used to achieve operation within a unitary power factor, along with a reduction in THD in the electrical grid due to the 5-leveled structure, thus improving the harmonic content. Synchronizing the proposed converter to the electrical network is done by using a UVG (Unit Vector Generation) that generates a reference angle for the transformer blocks used in the simulation. The operational results presented in Matlab/Simulink software.

## 2. CONFIGURATION OF THE PROPOSED THREE-PHASE CONVERTER TOPOLOGY

The structure of the proposed converter was formed by replicating the single-phase topology presented in (Onar et al., 2012) applied to electric vehicle. Due to the phase symmetry, some aspects of the study conducted in (Rodriguez et al., 2002; Onar et al., 2012) are thus considered in the analysis of the three-phase converter version.

Figure 1 shows the new three-phase NPC converter proposed in this paper. The semiconductors $S_{ai}$ with $i = \{1, 2, 3, 4\}$, $S_{bj}$ with $j = \{1, 2, 3, 4\}$ and $S_{ck}$ with $k = \{1, 2, 3, 4\}$ are IGBT (Insulated Gate Bipolar Transistor) type transistors and have module phase A, B and C devices respectively. The diodes $D_{ai}$ with $i = \{1, 2, 3\}$, $D_{bj}$ with $j = \{1, 2, 3\}$ and $D_{ck}$ with $k = \{1, 2, 3\}$ represent the clamping diodes of module phase A, B, C, respectively. The capacitors $C_i$ with $i = \{1, 2\}$ are the DC-bus capacitors, midpoint of DC link capacitors and clamping diodes of each leg is connected to the neutral of the three-phase AC source. The converter being proposed here is connected to a grid via single-phase transformer $T_i$ with $i = \{a, b, c\}$ at the output of each module.

The dc bus is shared among the three phases, so that single-phase transformers (interface element) must be used in the ac side to increase the output voltage to a suitable level and provides galvanic isolation, making the system as a whole safer. The voltages $V_{sx}$ with $x = \{a, b, c\}$ are the instantaneous grid voltage of phase A, B and C. The resistances $R_{sx}$, inductances $L_{sx}$, and $L_x$ with $x = \{a, b, c\}$ are the resistance, the line inductance of phase A, B, C, and the output inductance of converter of each module, respectively. neutral of three phase AC source.

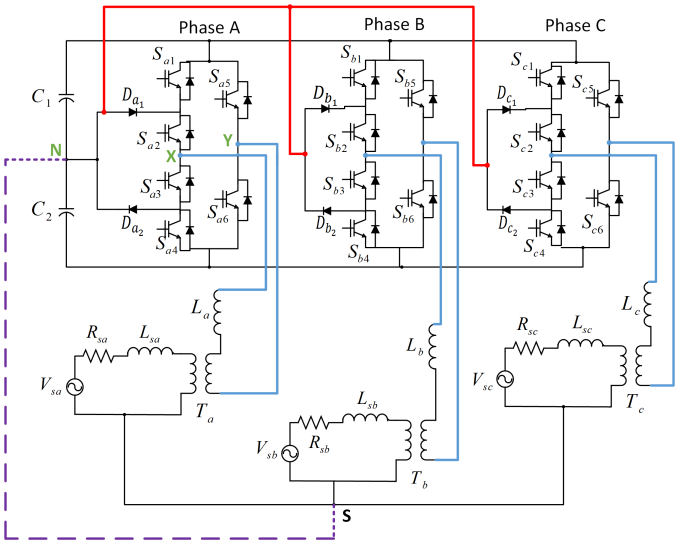


Figure 1. Topology of the proposed three-phase NPC. The point N and (X, Y) are the neutral point and the output of each module per phase.

## 3. STRATEGY OF PULSE WIDTH MODULATION (PWM) IMPLEMENTED

The converter operability is given by applying three different voltage levels at the point X (left side of the output inductor $L_a$) for phase A shown in Fig 1. Given this voltage and the commutation between the two voltage levels with the different pulse width in the added leg extension ($+V_{dc}$, $-V_{dc}$), it was obtained the output voltage waveform between the output points (X and Y). It is noteworthy that both legs are switching at different frequency, ie., the semiconductors $S_{ij}$ with $i = \{a, b, c\}$ and $j = \{1, 2, 3, 4\}$ switch in high frequency, while the semiconductors of the additional leg $S_{pk}$ with $p = \{a, b, c\}$ and $k = \{5, 6\}$ change state with the grid frequency.

Figure 2 shows the analog implementation of the modulation circuit used to properly activate the IGBTs in the converter shown in Figure 1. Sinusoidal modulation was chosen with various modulating signals i.e. one single sinusoidal signal was compared with four carriers in phase and offset in the y-axis.

Table 1 shows the different switching states of the semiconductors. Observe in Table 1 that semiconductors $S_{w1}$ and $S_{w4}$, located in the extreme end of the left leg of each module of the converter, only switch between two voltage levels (0, $\pm V_{dc}$). The semiconductors located on the additional leg, i.e. $S_{w5}$ e $S_{w6}$, switch in function of the half cycle of the grid i.e. $S_{w6}$ in the positive half cycle, and $S_{w5}$ in the negative half cycle.

Figure 3 shows the modulator with offset carriers in the y-axis. Variables $V_{trij}$ with $j = \{1, 2, 3, 4\}$ represent the carriers, and $m_o$ the reference signal (modulator).

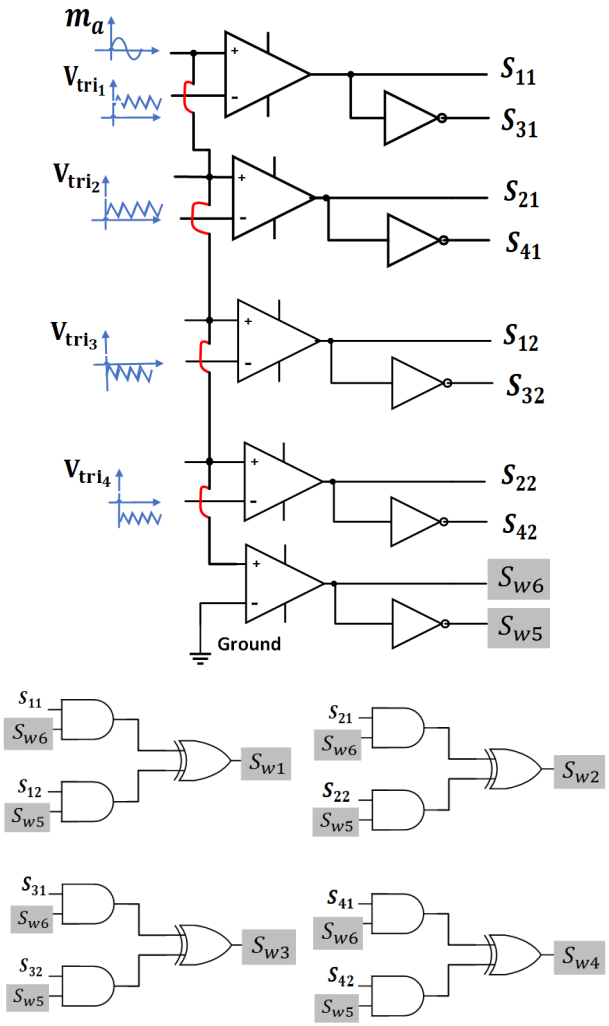


Figure 2. Analog implementation of PWM of only one phase. $S_{wm}$ with $m = \{1, 2, 3, 4, 5, 6\}$ are the generated pulses for one phase, $S_{rn}$ with $r = \{1, 2, 3, 4\}$ and $n = \{1, 2\}$ representing intermediate variables.

Table 1. States of the semiconductors

| Sates | $V_{ab}$ | $S_{w1}$ | $S_{w2}$ | $S_{w3}$ | $S_{w4}$ | $S_{w5}$ | $S_{w6}$ |
|---|---|---|---|---|---|---|---|
| 1 | $+V_{dc}$ | 1 | 1 | 0 | 0 | 0 | 1 |
| 2 | $-V_{dc}$ | 0 | 0 | 1 | 1 | 1 | 0 |
| 3 | $+V_{dc}/2$ | 0 | 1 | 1 | 0 | 0 | 1 |
| 4 | $-V_{dc}/2$ | 0 | 1 | 1 | 0 | 1 | 0 |
| 5 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 6 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

One can observe that a comparison between the modulator signal $m_o$ and the carriers $V_{trij}$ is insufficient, and does not allow for obtaining the necessary pulses to activate each semiconductor. Additional logic is thus necessary, as shown in Figure 2 that monitors the semi cycle in which the grid is operating to suitably switch the IGBTs.

Figure 4 shows the pulse signals generated to activate each one of the IGBTs of each module.

## 4. EMPLOYED CONTROL FOR THE PROPOSED CONVERTER

To ensure a functionality between the converter proposed and the grid, two points are discussed in this section.

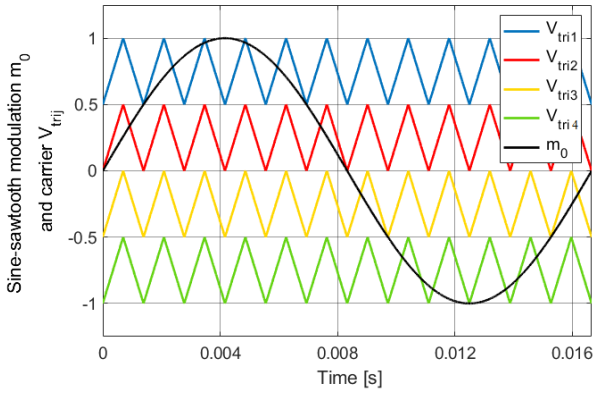


Figure 3. Modulator $m_o$ with $V_{trij}$ carriers offset from the y-axis.

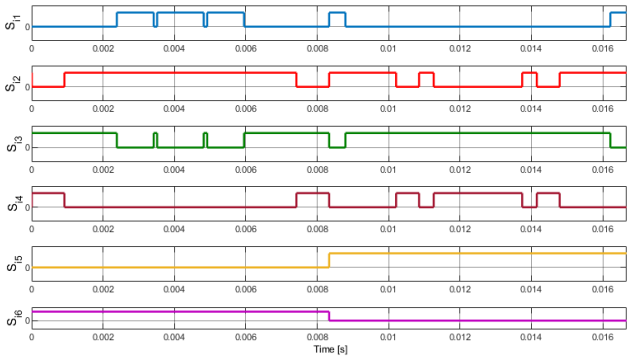


Figure 4. Waveform of the pulses to activate the IGBTs.

- The DC-link voltage is controlled in order to maintain it constant, and in turn controlling the flow of power.
- The output current in the transformers is controlled at each module per phase.

To meet these objectives, DQ synchronous reference frame vectorial control was used according to (Prasad et al., 2008). Vectorial control is a popular method for controlling three-phase induction motors to control flow and torque components produced in the current of the motor. This method is used at the point where the proposed converter is connected to the grid.

### *4.1 Mathematical Analysis of the DQ Synchronous Reference Frame Vectorial Control Applied to the Proposed Converter*

The grid voltages $V_{sx}$ with $x = \{a, b, c\}$ are transformed via (1) in two components $V_a$ e $V_b$, which are the components of the vector voltage $\overrightarrow{V_s}$ in the stationary reference structure shown in Figure 5.

$$\begin{bmatrix} V_a \\ V_b \end{bmatrix} = \begin{bmatrix} 3/2 & 0 & 0 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (1)$$

From (1) it is possible to transform components $V_a$ and $V_b$ in the DQ synchronous reference frame. This transformation is performed through the equation (2).

$$\begin{bmatrix} V_{sq} \\ V_{sd} \end{bmatrix} = \begin{bmatrix} -\sin(\theta) & \cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \end{bmatrix} \quad (2)$$

where:
$\theta$ - Angle between d-axis and a-axis.

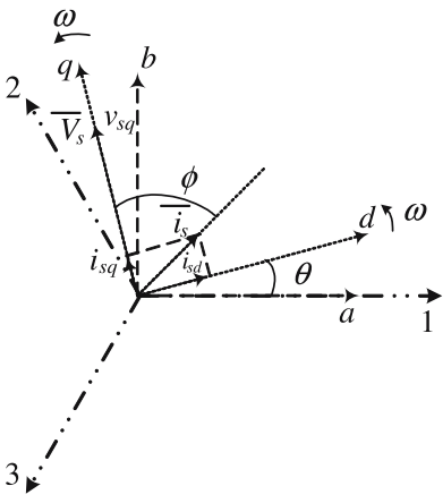


Figure 5. Vectorial diagram of the DQ synchronous reference frame.

### *4.2 Unit Vector Generation*

Traditionally, connecting a three-phase converter to the grid implied the need to synchronize it with the grid. The strategy usually employed to perform this has been the Phase Locked Loop (PLL) function. Many studies have been conducted using the PLL methodology (Abdalrahman et al., 2012; Krievs et al., 2010; Chung, 2000). In this paper the UVG method is used given its simplicity in generating unity vectors ($\sin(\theta)$ and $\cos(\theta)$) (Chung, 2000).

The angle between the vector voltage $\overrightarrow{V_s}$ and the a-axis shown in Figure 5 is equal to $\omega t$. One can offset $V_a$ (or $V_b$) by 90° using two first order low pass filters whose cut-off frequency is equal to that of the grid. The output of the filter $\alpha$ and $\beta$ shown in Figure 6 can be expressed via (3). Unit vectors $\cos(\theta)$ and $\sin(\theta)$ generated by the UVG necessary for the transformation into (2) are shown in (4).

$$\begin{aligned} \alpha &= \frac{3}{4}\sqrt{2}V_s\cos(\omega t - \frac{\pi}{2}) \\ \beta &= \frac{3}{4}\sqrt{2}V_s\sin(\omega t - \frac{\pi}{2}) \end{aligned} \tag{3}$$

$$\begin{aligned} \cos(\theta) &= \frac{\alpha}{\sqrt{\alpha^2+\beta^2}} \\ \sin(\theta) &= \frac{\beta}{\sqrt{\alpha^2+\beta^2}} \\ \theta &= \omega t - \frac{\pi}{2} \end{aligned} \tag{4}$$

### *4.3 Schematic Control Diagrams*

Control strategy for the proposed converter is implemented to ensure operation for obtaining a unitary power factor, as well as to improve the power quality. Figure 7 and 8 both show this control diagram.

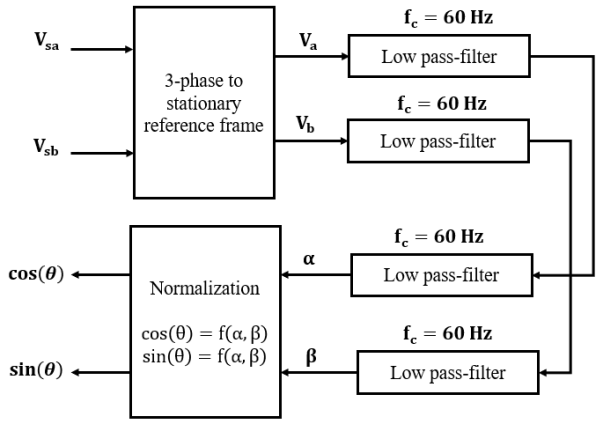


Figure 6. Unit Vector Generation. $\alpha$ e $\beta$ are intermediary variables, $f_c$ is the cut-off frequency of the filter.

The PRP regulator (Potential of the Reference Point), the DC-link voltage controller, the grid current controller, the PWM modulation block and the UVG constitute the principle modules of the schematic control diagram. The voltage controller is used to control the flow of power from AC and DC.

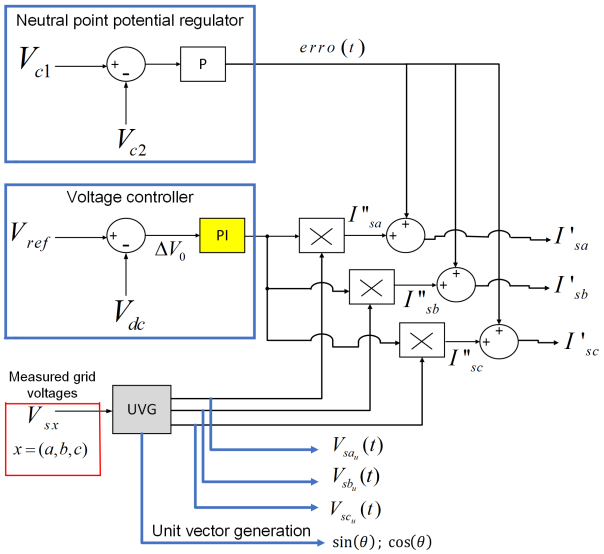


Figure 7. Voltage controller, Potential of the Reference Point, and the synchronization with the grid using UVG.

The amplitude of the line current can be expressed by (5).

$$\begin{aligned} I_m &= K_{pc}\Delta V_0 + K_{ic}\int \Delta V_0 \\ \Delta V_0 &= V_{ref} - V_{dc} \end{aligned} \tag{5}$$

where:
$I_m$ - Amplitude of the line current;
$K_{pc}$ - Proportional gain of the current controller;
$K_{ic}$ - Integral gain of the current controller;
$\Delta V_0$ - Error between $V_{ref}$ and $V_{dc}$;
$V_{ref}$ - Reference voltage for the voltage controller;
$V_{dc}$ - Measured voltage at the output of the voltage sensor put on the DC-bus.

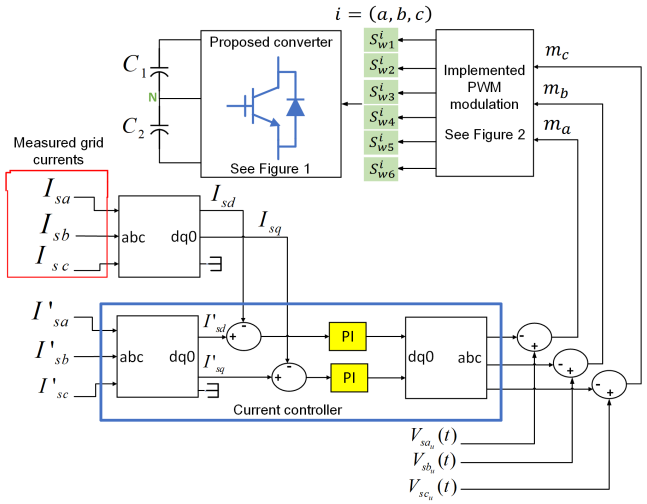


Figure 8. Current controller and PWM signal generator. $m_i$ with $i = \{a, b, c\}$ are the reference signals for the phases A, B and C.

The UVG block output creates sinusoidal voltages with amplitude equal to 1 and can be expressed by (6).

$$\begin{aligned} V_{sa_u}(t) &= \cos(\theta) \\ V_{sb_u}(t) &= \cos\left(\theta - \frac{2\pi}{3}\right) \\ V_{sc_u}(t) &= \cos\left(\theta + \frac{2\pi}{3}\right) \end{aligned} \tag{6}$$

The reference signals for the line currents are simply derived from the product of the output of the voltage controller with the unitary sinusoidal voltages. The obtained result from this block, shown in Figure 7, is added to the PRP output. Equation (7) shows the line current commands.

$$\begin{aligned} I''_{sa}(t) &= I_m \cos(\theta) \\ I''_{sb}(t) &= I_m \cos\left(\theta - \frac{2\pi}{3}\right) \\ I''_{sc}(t) &= I_m \cos\left(\theta + \frac{2\pi}{3}\right) \end{aligned} \tag{7}$$

The measured line currents and the referent currents are transformed in d-q using equation (2) before feeding the current controller in order to monitor the grid current commands. By not considering the commutation terms in high frequency, or rather, by only considering the fundamental components of the grid, one can express the grid voltage for phase A using (8).

$$V_{sa}(t) = \left[L_{sa}\left(\frac{N_s}{N_p}\right)^2 + L_a\right]\frac{\mathrm{di_{sa}(t)}}{\mathrm{d}t} + R_{sa}i_{sa}(t) + m_a(t) \tag{8}$$

where:
$L_{sa}$ - Inductance of the line of phase A;
$R_{sa}$ - Resistance of line of phase A;
$V_{sa}$ - Instantaneous voltage of the grid for phase A;
$i_{sa}$ - Instantaneous current of the grid for phase A;
$L_a$ - Inductance at the output of the module for phase A;
$m_a$ - Modulated control signal coming from the circuit in a closed loop system;
$N_s$ - Number of secondary windings in the transformer;
$N_p$ - number of primary windings in the transformer.

## 5. SIMULATION RESULTS AND DISCUSSION

As was mentioned in section 2, the proposed converter is connected to the grid using isolating single-phase transformers with a power rating of 2 kW each. The three-phase converter was simulated using Matlab/Simulink software. Two resistances, $R_1$ and $R_2$ with a value equal to 10 Ω connected in parallel via capacitors $C_1$ and $C_2$, respectively, are taken as a load when the converter is operating as a rectifier. Otherwise, resistance $R_1$ and $R_2$ are connected across the DC link capacitors to include loading effect of active front end converter (Chaturvedi et al., 2016). A current source with amplitude equal to 20 ADC was applied to the DC-bus when the converter was acting as an inverter. Table 2 shows the power circuit specifications. To calculate the value of the input capacitors and the inductance at the converter output of each module per phase shown in Figure 1, variations in the DC-link voltage $\Delta V_{dc}$ and in the inductance current $\Delta i$ are considered and are shown in Table 2. The transformer parameters are determined by short circuit and no-load tests.

Table 2. Power circuit Parameters

| Parameters | Value |
|---|---|
| RMS line voltage (V) | 220 |
| Line inductance (mH) | 0.427 |
| Output inductance of each module (mH) | 2.161 |
| Line resistance (Ω) | 0.2 |
| Total DC-bus voltage ($V_{C_1} + V_{C_2}$) (V) | 100 |
| Input capacitor (mF) | 53 |
| Switching Frequency (kHz) | 15 |
| Modulation Index | 0.778 |
| Active power of converter (kW) | 6 |
| Grid frequency (Hz) | 60 |
| DC voltage variation | 3% |
| AC current variation | 6% |
| Transformer power (kW) | 2 |
| Primary resistance (Ω) | 0.029 |
| Secondary resistance (Ω) | 0.433 |
| Primary inductance (μH) | 110.601 |
| Secondary inductance (mH) | 1.675 |
| Magnetizing resistance (Ω) | 3339 |
| Magnetizing inductance (H) | 1.464 |

The values of the PI controller (shown in Figures 7 and 8 ) parameters were obtained based on (Blasko and Kaura, 1997; Razali et al., 2014) and using the symmetrical optimum method (Leonard, 1976). Table 3 shows the controller specifications.

Table 3. PI Controller Parameters

| **Current Controller** | |
|---|---|
| Parameters | Value |
| Proportional gain $K_{pc}$ | 2.734 |
| Integral gain $K_{ic}$ | 15189 |
| **Voltage Controller** | |
| Proportional gain $K_{pv}$ | 18.31 |
| Integral gain $K_{iv}$ | 678.02 |

Figure 9 shows the waveforms for $\cos(\theta)$ and $\sin(\theta)$ generated by the UVG based on Figure 6.

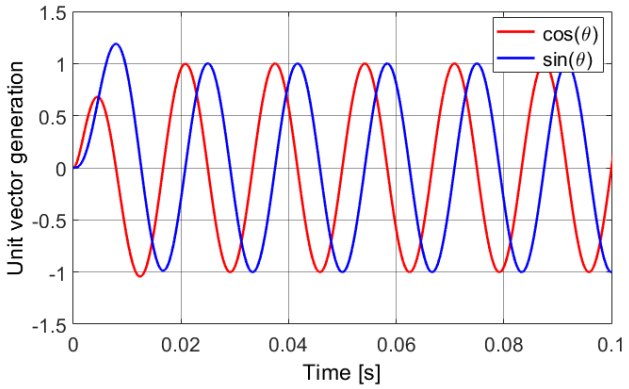


Figure 9. Unit Vector Generation (UVG).

Figure 10 shows the waveforms of the phase A mains AC voltage $V_{sa}$ and current $i_{sa}$. One can see that the grid voltage and current are in phase when the proposed converter is operating as a rectifier. In order to prove the dynamic effect of the proposed system, t = 0.2 s was applied with a resistive load of $(R'_1, R'_2) = 10\ \Omega$ in parallel to the existing load $(R_1, R_2) = 10\ \Omega$. The grid current $i_{sa}$ remains in phase with the grid voltage and results in a THD value equal to 1.41% shown along its harmonic spectrum in Figure 11.

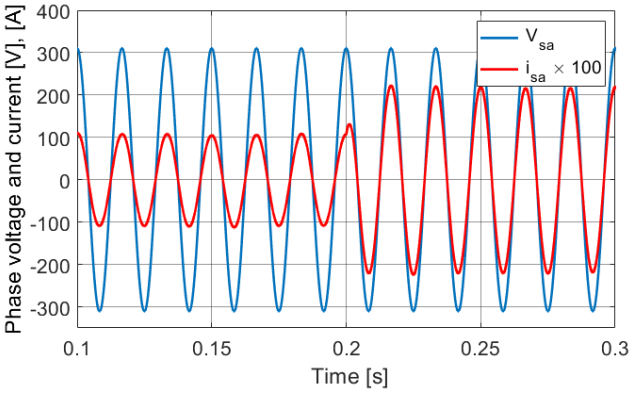


Figure 10. Grid voltage $V_{sa}$ and current $i_{sa}$.

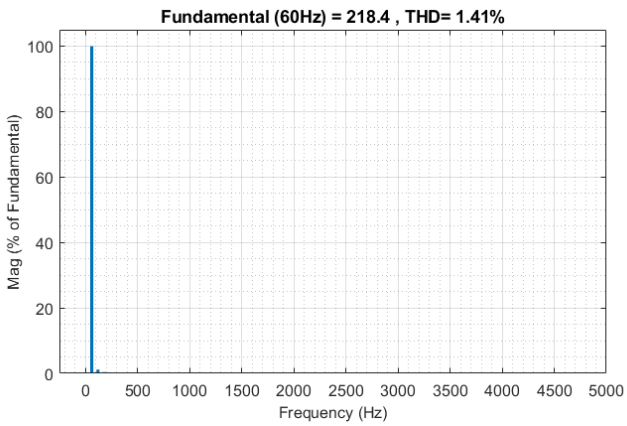


Figure 11. Harmonic spectrum of grid current $i_{sa}$ (rectifier mode).

Figure 12 shows the total DC-link voltage $(V_{C_1} + V_{C_2})$. Note that the DC voltage maintains its applied reference value $V_{ref}$, shown in Table II. Thus, the voltage controller performs efficiently.

The resistive load was substituted by a current source with amplitude of 20 ADC. To once again prove the dynamic effect of the inverter t = 0.2 s was applied with a variation of 80% in the current, and after that instant a maximum current was then applied.

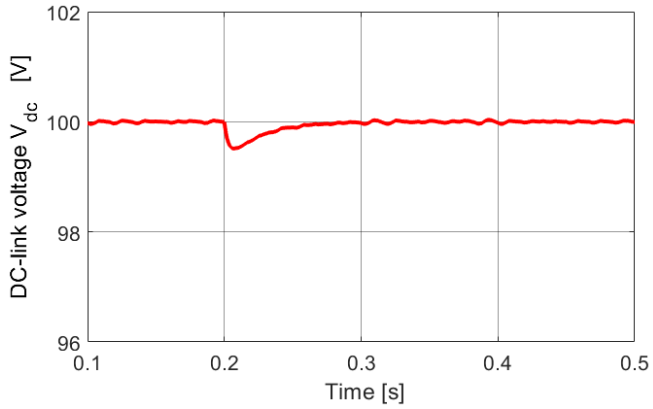


Figure 12. DC-link voltage $V_{dc}$.

Figure 13 shows the source voltage $V_{sa}$ and current $i_{sa}$ of phase A, and the input single-phase transformer voltage. One can see that the input transformer voltage has five desirable levels and is thus more advantageous with respect to the conventional three phase three-level NPC since a classic NPC has three levels of AC voltage per phase. The grid current $i_{sa}$ in Figure 13 has a THD approximately equal to 1.81%, changes amplitude after t = 0.2 s, and is in counter phase with grid voltage $V_{sa}$ when the proposed converter is operating as an inverter.

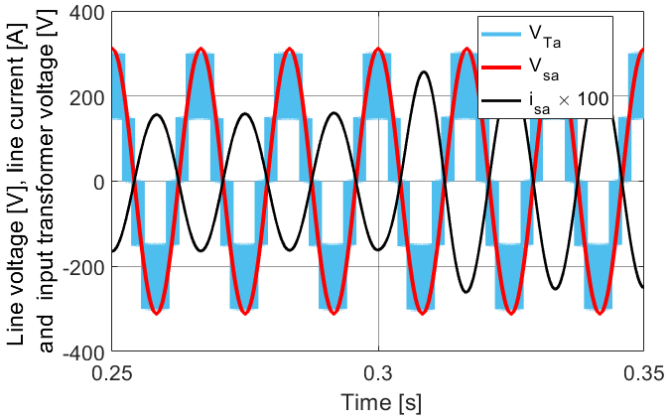


Figure 13. Grid voltage $V_{sa}$ and current $i_{sa}$ and input transformer voltage $V_{T_a}$ in phase A.

## 6. CONCLUSION

The proposed converter is connected to the electrical grid via single-phase transformers at the output of each phase module. This converter was simulated in Matlab/Simulink software using DQ synchronous reference frame vectorial control. The UVG method was used for its simplicity of implementation to substitute the traditional PLL method and to detect the reference angle for the transformer blocks

used in the simulation. The obtained results show that the proposed converter is functionally dynamic because the grid current is in phase with the voltage and has a THD equal to 1.41% when the converter is operating as a rectifier. When the grid current is in counter phase with the voltage, the THD is equal to 1.81% when the proposed converter is acting as an inverter. The THD values obtained in both the cases mentioned above are within the IEEE 519 limitations (Duffey and Stratford, 1989). The DC-link voltage was controlled and maintained practically constant at its reference value. The proposed converter has five voltage levels at the output for each phase, which has proven more advantageous than the conventional three-phase NPC converter given that the AC voltage per phase in the conventional three-phase NPC topology has three voltage levels.

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