A New Limited Switching Frequency Digital Hysteresis Current Control Strategy for a Five-Level Medium Voltage Induction Motor Drive

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Abstract: This paper presents a new limited switching frequency digital hysteresis current control method for a five-level neutral point clamped (NPC) Type G medium voltage induction motor drive. An indirect rotor field-oriented controller (RFOC) is used to speed control. The hardware topology and the controller implementation are described. The proposed method is compared to the traditional one, which is based on sampling frequency limitation. Results obtained from computer simulations are presented. It can be noted from them an improvement of the voltage and current harmonics spectra and diminution of the torque ripple amplitude.

Keywords: Multilevel inverter; current control; hysteresis; neutral point clamed (NPC); pulse width modulation (PWM).

1. INTRODUCTION

With the advancement of industrial automation, AC machines need more effective control, allowing better control of speed, acceleration and torque, in addition to better efficiency. For this reason, power converters must have better strategies to optimize their operation, as is the case of those that use PWM modulation techniques.

The PWM converter with current control has some advantages on standards PWM, like overload rejection, good dynamics, peak current protection, compensation of load parameters change, semiconductor voltage drop and dead times of the converter (Kazmierkowski & Malesani, 1998). This is the reason for using current control in high performance drives.

The performance of the converters depends on the applied current control strategy. The voltage source inverters (VSIs) current control techniques can be categorized as linear or non-linear. Some non-linear controllers are based on hysteresis strategies that, in spite of operate with variable frequency (Novotny & Lipo, 1996), provides a fast response to transient events (Bode & Holmes, 2000) (Jena, et al., 2011).

The hysteresis regulator is the simplest type of PWM current regulator. Despite its good current amplitude control, the highly variable switching rate may cause low frequencies to appear in the spectrum (Novotny & Lipo, 1996). Even so, hysteresis control offers fast response and good accuracy, besides less dependency on load parameters. These and other benefits of hysteresis modulation have renewed interest in studding this technique as seen recently in (Elnady & Nasir, 2022), (Lakhimsetty, et al., 2019), (Shah, et al., 2020), (Chakraborty & Dey, 2020), (Kubera, et al., 2016), (Raju, et al., 2019), (Ejlali, et al., 2016), (Ramos, et al., 2020), and others. In order to take advantage of these benefits, this work makes use of the hysteresis current control technique to control a five-level medium voltage drive.

The main motivation for doing this work is some of the difficulties commonly faced to implement indirect rotor field-oriented control (RFOC) in medium voltage drives. As is well known, slow switching devices such as those used in this type of drive lead to low actuation rates (Mohan, et al., 1989), which causes delays in command synthesis and errors in the field orientation angle. An awkward compensation of this angle is necessary if a linear current control is used because it requires the implementation of a voltage decoupler. It calculates voltage references from current references and machine model parameters. The inherent delay in the voltage commands synthesis and errors in the machine model estimated parameters cause incorrect field orientation, impairing the controller's performance. Thus, techniques such as hysteresis current control are extremely welcome to this application, as they synthesize current commands directly and therefore do not require voltage decoupling. Therefore, the computational efforts, as well as the error caused by the variations of the machine parameters are reduced.

In the hysteresis control, when the current slope varies, the inverter switching frequency may become too high, exceeding the semiconductor devices limits. This paper proposes a way to overcome this problem, limiting the switching frequency by delaying the switches commands in some circumstances. This method is compared to the traditional one which seeks to limit this frequency through the sampling frequency used on the controller.

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Presently, the control circuits of modern converter tend to be digital, what is possible with the use of Digital Signal Processors (DSPs). This paper proposes the implementation of a digital hysteresis current control with the use of a Field-programable Gate Array (FPGA) in addition to the DSP, sharing computing efforts and allowing an asynchronous signal processing. Analog hysteresis has been successfully and widely implemented, but digital hysteresis, on the other hand, has some challenges to be overcome (Yi, et al., 2016).

This paper is organized as follows: Section 2 introduces briefly the five-level NPC Type G inverter topology chosen for this study. Section 3 presents the basic operation of current hysteresis and the multiband method used on multilevel inverters. Section 4 proposes the multiband method with the addition of the switching frequency limiter improving its performance. Section 5 gives simulations results to check effectiveness of proposed technique. Finally, conclusion of this paper is summarized in Section 6.

2. INVERTER TOPOLOGY

In medium voltage inverters, there is an intrinsic problem of the operation in high frequencies due to semiconductors limitations. Another problem comes from high dv/dt commutation and high voltage that needs to be blocked by the switches. One way to solve this is the use of multilevel topologies, which divides the effort of each switch, allowing the inverter to operate in high power systems, besides improving the THD in drive's output voltage. The topology chosen for this study is the NPC Type G inverter (Hill & Harbourt, 1999), which shows itself very suitable for many modulation strategies. In NPC Type G, each phase uses two legs of a common 3-level NPC, as shown in Figure 1. The complete scheme is shown in Figure 2. In this circuit the three power modules are connected in a common neutral point, and a wye-delta-zig-zag transformer is used to reduce the harmonic content of rectifiers input current.

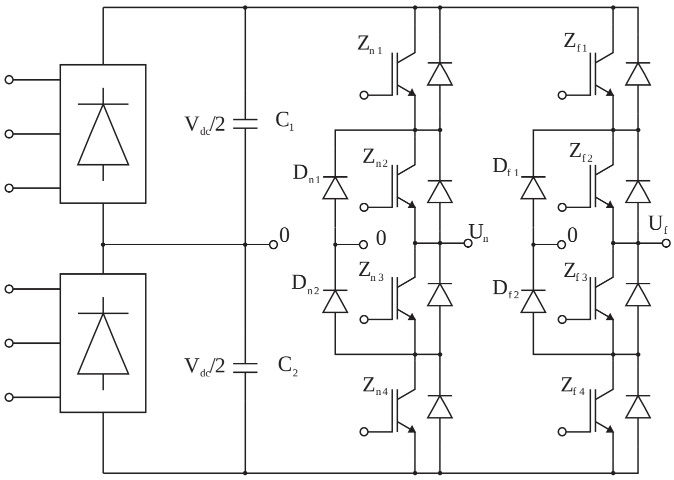

Figure 1 – Power module based on three-level NPC legs *(Luiz & Stopa, 2015).*

In this topology it is possible to obtain five-levels in the inverter's output phase voltage. A 5-level NPC converter has 60 active space vectors, what leads to 9 steps in the line-to-line voltage.

Increasing the number of voltage levels increases the complexity of implementing the modulation technique. In this paper hysteresis current-regulation is applied in NPC Type G converter and this technique is detailed in the following sections.

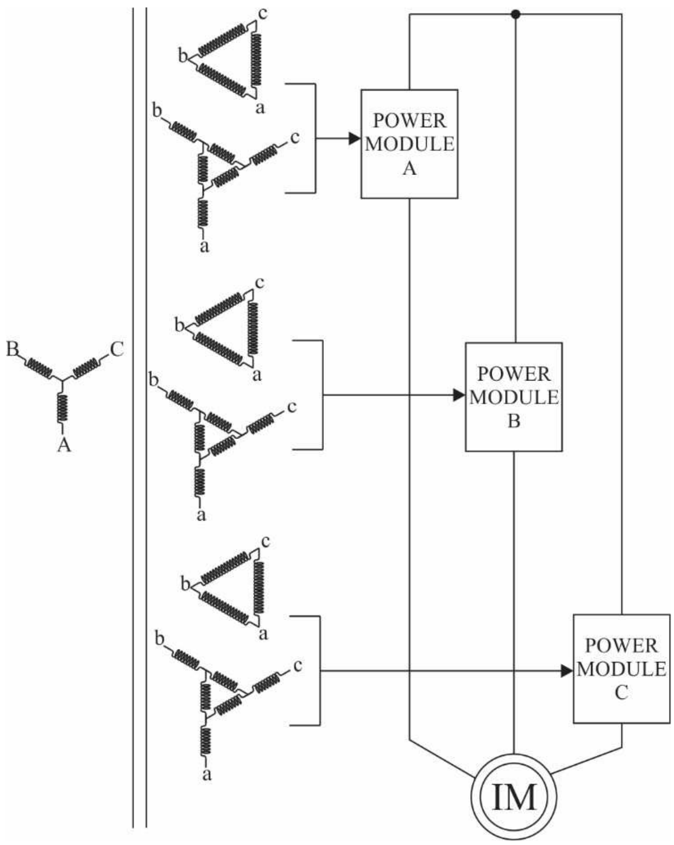

Figure 2 – A five-level NPC Type G inverter *(Luiz & Stopa, 2015).*

3. HYSTERESIS CURRENT-REGULATION

The PWM hysteresis current regulator consists of a reference current signal that is compared to the measured current, generating an error signal. This signal is applied to a hysteresis comparator producing the logical commands to the switches. Figure 3 shows the typical hysteresis regulator behavior.

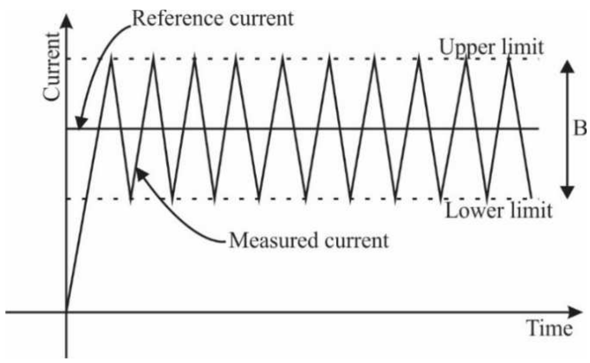

Figure 3 – Typical hysteresis regulator behavior.

In Figure *3* the hysteresis band B determines current limits, and, when the upper limit is reached the control logic acts combining the switches states so that the current starts to decrease. Otherwise, when the current reaches the lower limit,

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the control logic acts in the opposite way, causing the current to increase again and the cycle repeats continuously. On a multilevel inverter, the control logic is more complex and have multiple ways to be implemented. Section 3.1 describes one of these methods.

3.1 Multiband Hysteresis Current Regulation

Some control methods for current hysteresis in multilevel converters have been proposed, as in (Bode, et al., 2001)-(Marchesoni, 1989). The main methods were compared in (Shukla, et al., 2011), where the multiband method, first proposed in (Marchesoni, 1989), proved to be efficient and easy to implement, which is why it was selected for this study.

The multiband hysteresis operation is illustrated in Figure 4. In this case there are outer bands ΔB in addition to the inner band B. When the error touches the inner band, the inverter switches in adjacent voltage levels. When an outer band limit is reached, an additional level is selected. The hysteresis control system is shown in the Figure 5, where the reference current is compared to the measured current generating an error signal. This signal is applied to hysteresis elements, one for the inner band and one for each outer band. The outer bands generate pulses through monostable vibrators for a counter that defines which levels will be used. The system uses three independent controllers, which means that each phase has its own hysteresis control system. If the control logic is efficient enough, the load will have to be fed only by the necessary voltage levels. In the case of an induction motor with near to zero speed, for example, the lowest voltage levels can be used by the 5-level inverter, as well as a 3-level inverter. This helps in the synthesis of the output voltage, improving the V/f ratio, decreasing switching losses and decreasing the dv/dt variation, which reduces the effort of the switches.

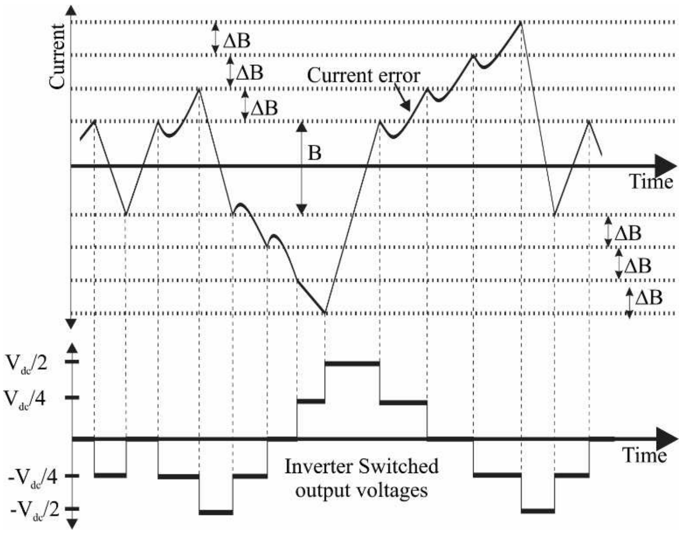

Figure 4 – Multiband five-level hysteresis current control *(Shukla, et al., 2011)*.

4. MULTIBAND HYSTERESIS WITH SWITCHING FREQUENCY LIMITER

In digital hysteresis current control, the reference is sampled, so the maximum switching frequency is limited to a half of the sampling rate (Ramos, et al., 2020). It happens because the inverter acts just once at a sampling time period. This is often used to set the converter maximum switching frequency. In the multiband hysteresis, if the current varies very quickly, the error can cross more them one outer band, causing the output voltage to change abruptly through multiple levels. This behavior is illustrated in the Figure 6 example, where T_a and T_b are two different sampling times. Note that T_b is four times larger than T_a, causing the output voltage to change more levels if compared to T_a case.

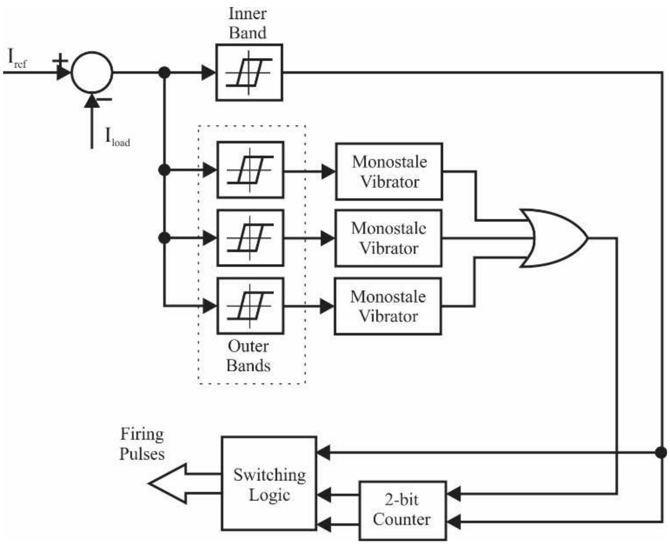

Figure 5 – Multiband hysteresis control system for each phase.

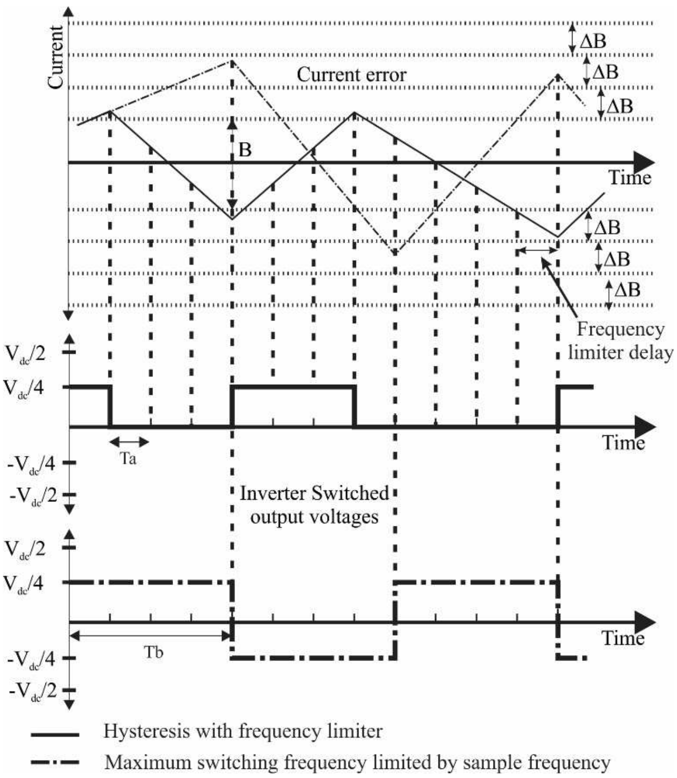

Figure 6 – Digital multiband hysteresis behavior.

Another way to establish a maximum switching frequency is through the use of a frequency limiter on firing pulses signals. In this way, the sampling frequency may be higher, making the circuit respond better (more quickly) to hysteresis commands. Figure 6 shows the difference between two cases. Case 1 is the

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conventional digital hysteresis and case 2 is the hysteresis with the frequency limiter. In case 1 the sampling time T_b is four times larger than T_a (case 2). It can be noted that in case 1 the current error reaches the outer hysteresis band before the next sample. It causes the output voltage to change abruptly through two levels. It does not occur in case 2, in which only two voltage levels are used. It happens because of the faster acting of the converter in case 1, that was provided by the smaller sampling time. In Figure 6 it can be noted the frequency limiter acting on the last switching in case 1 (sample time = T_1), when the turn on pulse is delayed. In both cases, maximum switching frequency is given by $1/(T_b+T_b)$.

Figure 7 shows the scheme for the proposed frequency limiter. Monostable vibrators are used to count the corresponding period of time of the frequency limit. It receives a positive pulse on the input and generates a fixed width pulse on the output. The flip-flop holds the output until the monostable allows it to change again.

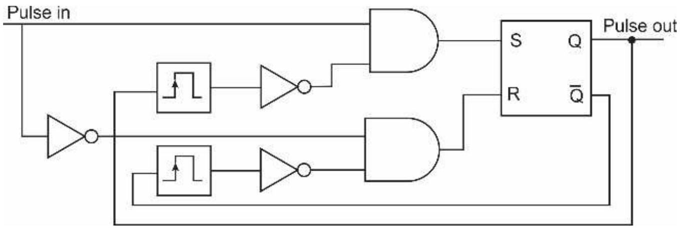

Figure 7 – Frequency limiter.

In the case of hardware implementation, a speed control and the hysteresis current control must operate in asynchronous mode in respect to the frequency limiter, since it will not depend on the control sampling rate, allowing more accurate firing pulses. This leads to the need of two different processing units as shown in Figure 8, in which a DSP is responsible for the speed control and the hysteresis current control, and a FPGA is responsible for the switching logic and the frequency limiters.

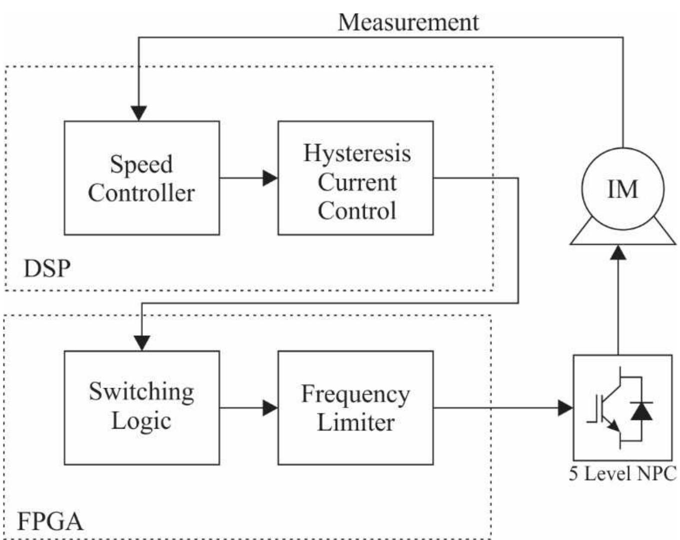

Figure 8 – Processing scheme of the system.

5. SIMULATION MODEL AND RESULTS

A simulation model is used to compare the traditional digital multiband hysteresis current control, using the sampling rate to control the maximum switching frequency, and the proposed method using the frequency limiter on firing pulses signals.

The system was implemented on PLECS® simulation software. It consists of the digital multiband hysteresis described before driving a 6,000 hp RFOC induction motor drive (Novotny & Lipo, 1996), as shown in Figure 9.

The machine used on the simulation is a 4-pole, 60 Hz, 3-phase induction motor, 6,000 hp, 4,160 V and 1,787 rpm rated speed. The inverter is a five-level Type G NPC with DC bus set to 3,400 V, and the maximum switching frequency considered is 2.5 kHz due to semiconductors limitations in this power range.

In order to speed up the flux establishment, it was used a flux control loop. It reduces the simulation time.

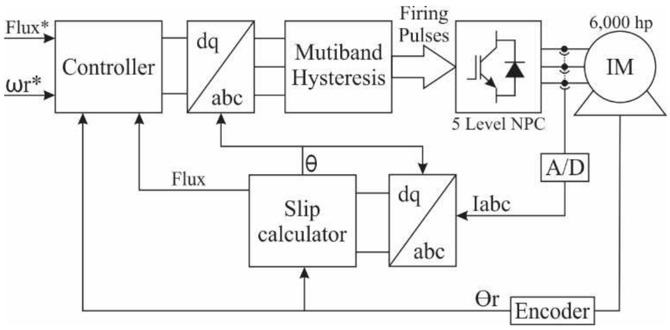

Figure 9 – System of a digital multiband hysteresis current control driving a 6,000 hp induction motor.

Two situations were simulated. Case 1 is the standard digital multiband hysteresis with the sampling frequency of 5 kHz, which gives a maximum switching frequency of 2.5 kHz. Case 2 is the multiband hysteresis with frequency limiter. The sampling frequency was set to 15,360 kHz and maximum switching frequency to 2.5 kHz.

The simulation starts by, first establishing the machine flux to its rated 8.89 Wb value, which occurs in 15 s. After that, a speed ramp reference is applied to the control with a final value corresponding to the machine nominal (1,787 rpm). A load step torque is applied at 20 s, again with the machine nominal value (23,900 Nm).

Figure 10 and Figure 11 show the motor speed and torque (estimated) in case 1 and 2, respectively. In case 1, the maximum torque ripple is 34,930 Nm, and 7,661 Nm in case 2.Figure 12 and Figure 13 show line to neutral voltage, line to line voltage and current harmonic spectrum for cases 1 and 2 in steady state operation. The rectangular time window was used to calculate the harmonic spectrum corresponding to one signal period.

It is noticed that in case 1, without frequency limiter and sampling frequency of 5 kHz, the torque oscillation is much higher than that in the second situation, with the frequency limiter and 15,360 kHz sample frequency, mainly at the beginning of the speed ramp (low speed operation). At this point, the counter emf is smaller, and for this reason, the

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current tends to vary faster, as can be seen in Figure 14. This problem is minimized in the second situation, as shown in Figure 15, where the sampling rate is higher and the commands tend to have a better response to hysteresis commands. With a low sample frequency, the inverter tends to cause abrupt changes in the output voltage (Figure 14 detail). The same occurs in steady state situation, as can be seen in Figure 16. Figure 17 shows the steady state condition with the frequency limiter and higher sample frequency, what avoids the abrupt changes in output voltage.

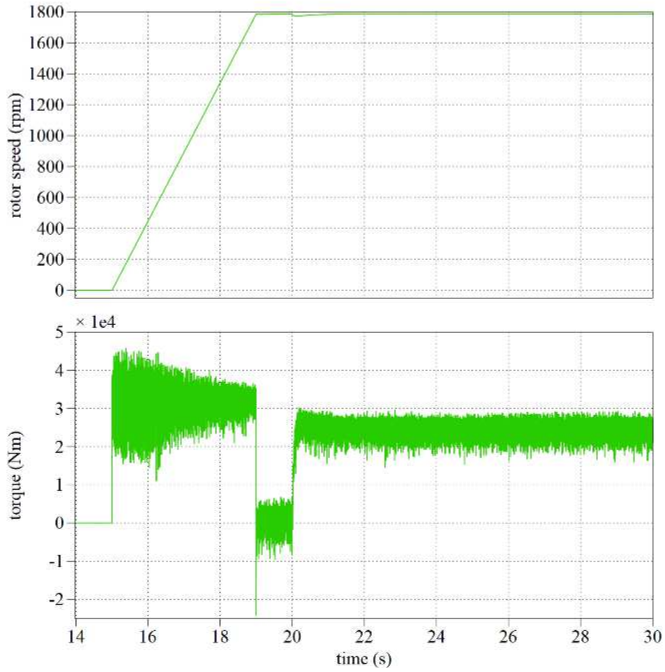

Figure 10 – Case 1: speed and electrical torque (estimated) of induction motor driven by multiband hysteresis without frequency limiter and 5 kHz sampling frequency.

Another important aspect to be observed is that in the second situation only the lowest voltage levels are used during the start of the induction machine (low speed operation). This is a more adequate behavior of the proposed multiband hysteresis control system.

It is important to note that, with the higher sampling frequency, the THD of the load voltage and current are much better, as can be seen in Table 1.

Table 1 – THD of the load voltage and current at steady state condition.

	THD (%)	
	5 kHz Sample frequency	15,360 kHz Sample frequency
Line to neutral voltage	44.4	34.0
Line to line voltage	36.8	23.8
Current	9.52	5.48

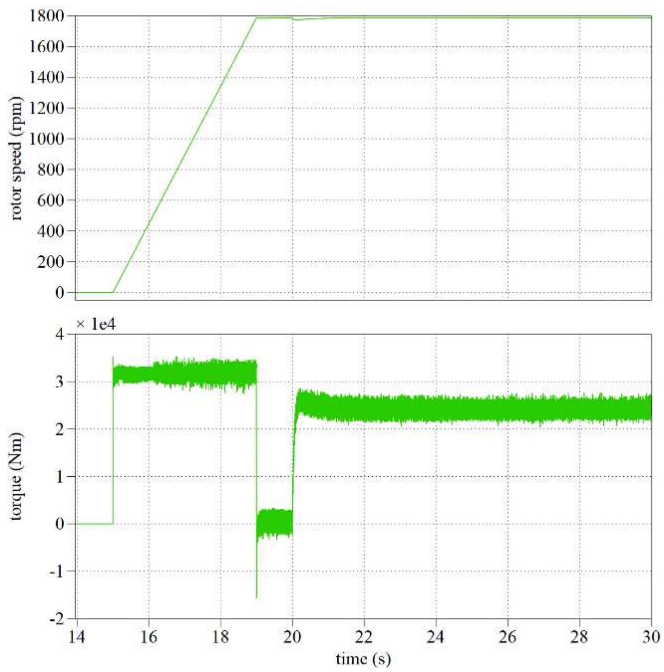

Figure 11 – Case 2: speed and electrical torque (estimated) of induction motor driven by multiband hysteresis with frequency limiter and 15,360 kHz sampling frequency.

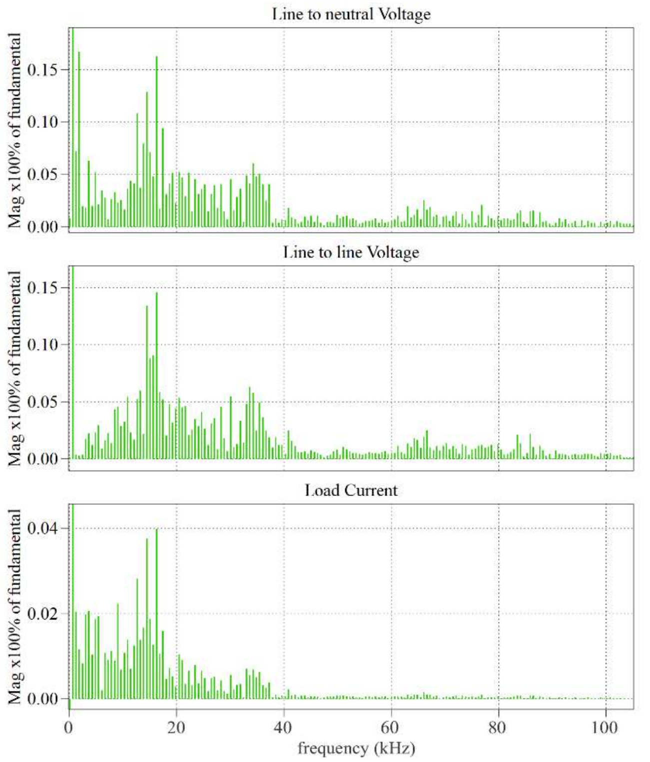

Figure 12 – Case 1: line to neutral voltage, line to line voltage and current harmonic spectrum for multiband hysteresis without frequency limiter and 5 kHz sampling frequency and steady state operation.

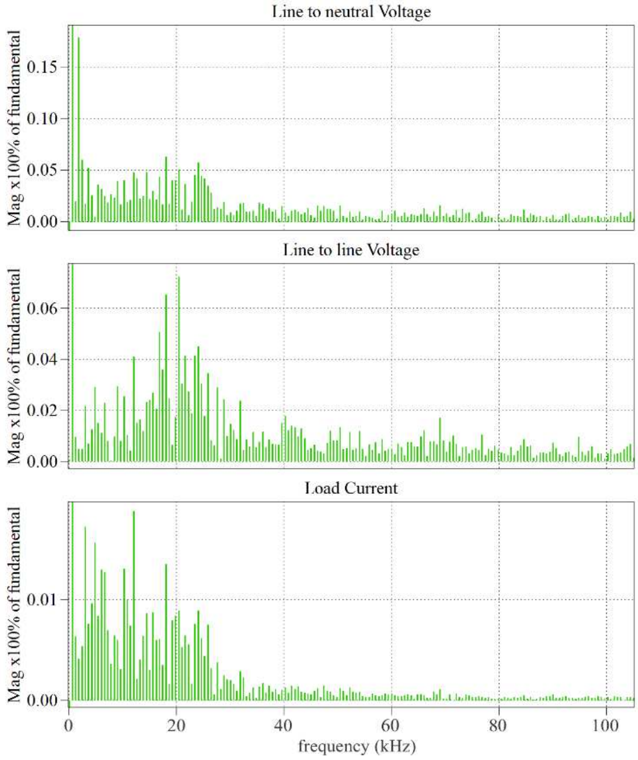

Figure 13 – Case 2: line to neutral voltage, line to line voltage and current harmonic spectrum for multiband hysteresis with frequency limiter and 15,360 kHz sampling frequency in steady state operation.

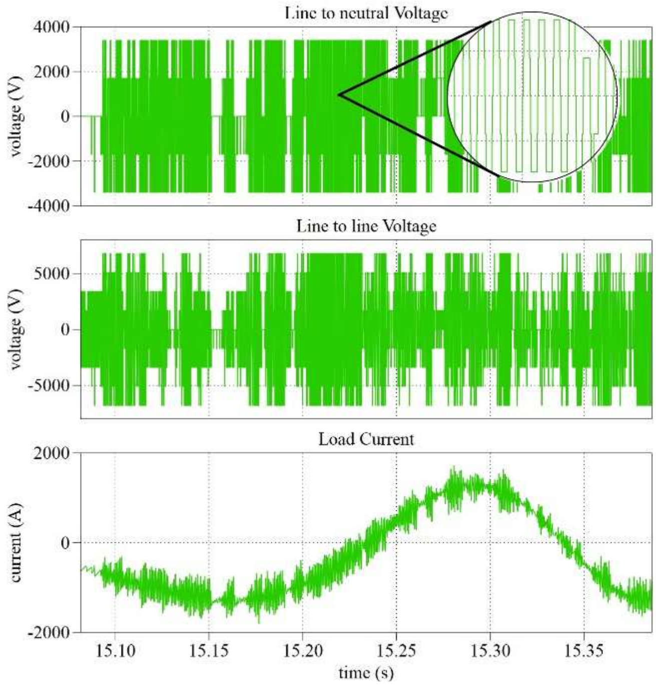

Figure 14 – Case 1: load voltage and current at the beginning of the speed ramp (low speed operation). Hysteresis without frequency limiter and 5 kHz sampling frequency.

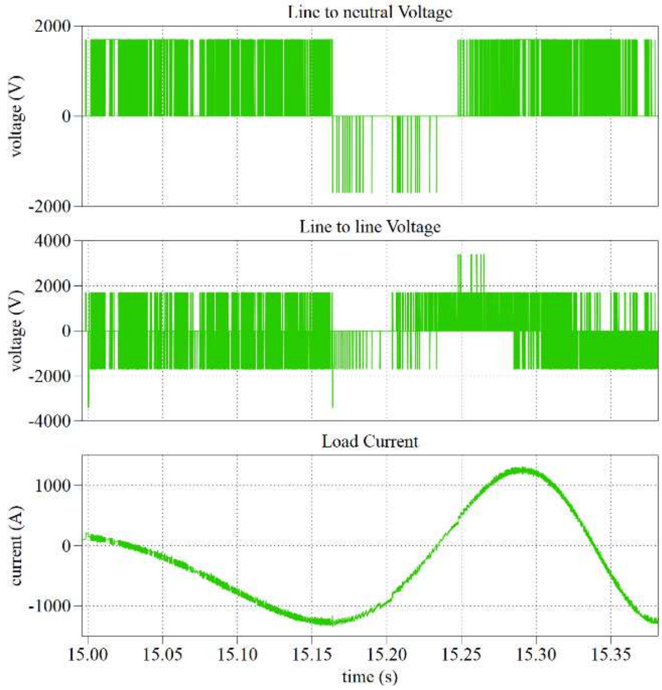

Figure 15 – Case 2: load voltage and current at the beginning of the speed ramp (low speed operation). Hysteresis with frequency limiter and 15,360 kHz sampling frequency.

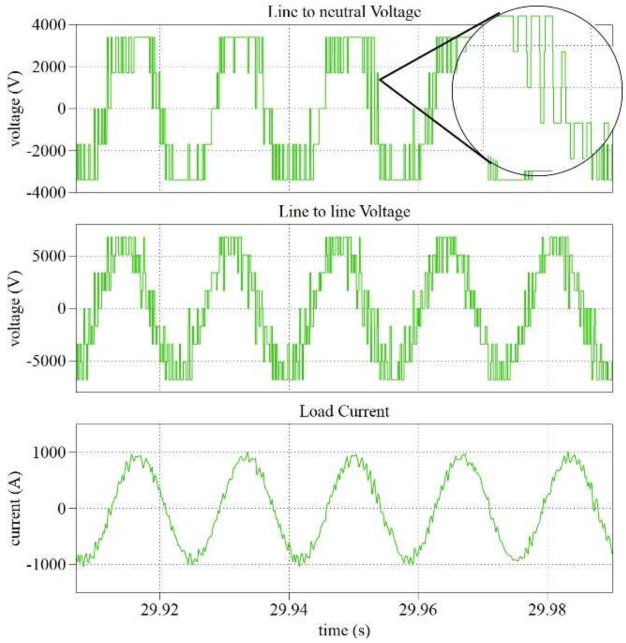

Figure 16 – Case 1: load voltage and current at steady state operation. Hysteresis without frequency limiter and 5 kHz sampling frequency.

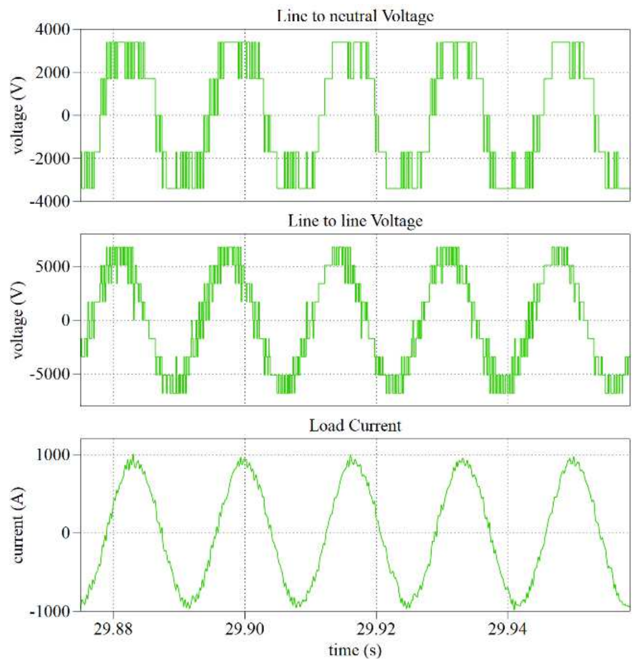

Figure 17 – Case 2: load voltage and current at steady state operation. Hysteresis with frequency limiter and 15,360 kHz sampling frequency.

6. CONCLUSION

After a short introduction of the NPC Type G inverter topology and hysteresis regulation, the paper presented a simple way to improve the performance of a digital multiband hysteresis current control in a medium voltage induction motor drive. The method consists of placing a frequency limiter on the converter firing pulses and increasing the control sampling frequency. To be implemented, the system must have two digital processing units operating asynchronously, as in the example presented, which uses a DSP and an FPGA. This method avoids abrupt changes in non-adjacent levels present in the conventional digital hysteresis method, which uses a low sampling frequency to limit the maximum switching frequency of the inverter. Besides that, the proposed method improves the output voltage and current harmonic content and decreases the torque ripple.

The NPC Type G inverter shows itself a good option for the proposed modulation method, ensuring smaller dv/dt variation (half the DC bus voltage) on the inverter output voltage and being able to work with higher voltages compared to the 3-level NPC.

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